(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 932 322 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.07.1999 Bulletin 1999/30

(51) Int Cl.[6]: **H04Q 11/04**

(21) Application number: **99101401.0**

(22) Date of filing: **26.01.1999**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **26.01.1998 JP 1285298**

(71) Applicant: **NEC CORPORATION**
Tokyo (JP)

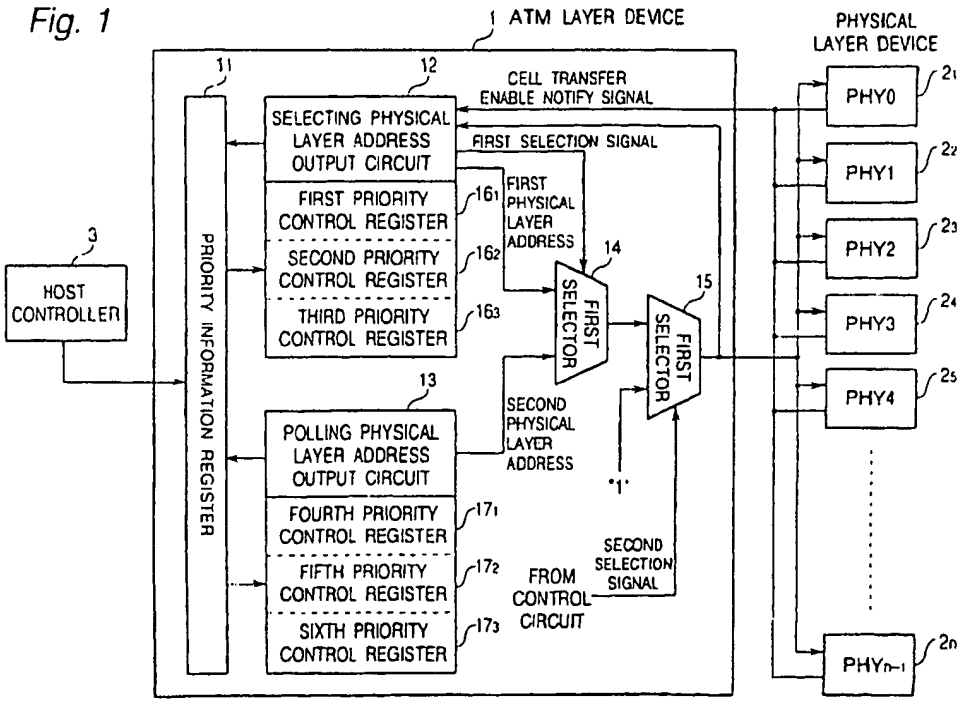
(72) Inventor: **Sudo, Eiji**
Minato-ku, Tokyo (JP)

(74) Representative: **Betten & Resch**
Reichenbachstrasse 19
80469 München (DE)

(54) ATM layer device controlling method and ATM layer device

(57) There is disclosed an ATM layer device configured to realize the function of an ATM layer by selecting one from a plurality of physical layer devices realizing the function of a physical layer, and executing a transfer of a cell, which is a unit of transmission, between the ATM layer device and the selected physical layer device. A priority information indicating the previously set priority level of each of said plurality of physical layer devices, is held and the physical layer device which should execute the cell transfer, is selected in a predetermined order in accordance with the priority information. Thus, the drop of the cell transmission rate and the overflow of a receiving buffer in the physical layer device are suppressed.

Fig. 1



EP 0 932 322 A2

Printed by Jouve 75001 PARIS (FR)

Description

Background of the Invention

Field of the invention

[0001] The present invention relates to an ATM (Asynchronous Tranfer Mode) layer device for realizing the function of an ATM layer in an ATM transmission network

Description of related art

[0002] In an ATM transmission network adopted in a B-ISDN and others, a protocol for transferring information is constituted of a plurality of layers. Respective layers have inherent functions, and one layer is realized by utilizing the function of a layer inferior to the first named layer by one layer.

[0003] Of the plurality of layers, a lower layer which is the most remote layer from a user's side, includes a physical layer and an ATM layer.

[0004] The physical layer is a layer for providing a resource for transferring a cell which is a unit of information-transmission, and specifically executes generation of a signal format suitable to a transmission medium, receiving of a signal, an encoding, or generation and elimination of a transmission frame. Furthermore, the physical layer checks whether or not the information included in the cell is effective, and transfers the cell carrying the effective information (effective cell) to the ATM layer.

[0005] The ATM layer is a layer superior to the physical layer by one layer, and executes a multiplexing and a separation of cells.

[0006] An ATM layer device which is a device realizing the function of the ATM layer and a physical layer device which is a device realizing the function of the physical layer, are connected through for example a UTOPIA interface (one of interface standards).

[0007] Fig. 7 is a block diagram illustrating the connection between the ATM layer device and the physical layer devices.

[0008] As shown in Fig. 7, to an ATM layer device 101, "n" physical layer devices 102_1 to 102n (where "n" is positive number) are connected through a UTOPIA interface. The ATM layer device 101 selects one from the "n" physical layer devices 102_1 to 102n, and transfers a cell between the ATM layer device and the selected physical layer device. Incidentally, the prior art ATM layer device gives an equal opportunity of selection to all the physical layer devices 102_1 to 102n, since the priority order is not provided among the physical layer devices 102_1 to 102n.

[0009] A system for equally selecting the physical layer devices 102_1 to 102n includes for example a round robin scheduling. In this round robin scheduling, as shown in Fig. 8, all the physical layer devices 102_1 to 102n are selected in a predetermined order as if a closed loop is depicted.

[0010] In the UTOPIA interface standard, on the other hand, since a transmission rate of the cell is not defined, a physical layer device having a high transmission rate and a physical layer device having a low transmission rate are connected to the ATM layer device in a mixed condition.

[0011] For example, consider a case that a plurality of physical layer devices having a low transmission rate exist and simultaneously receive the cell, and one physical layer device having a high transmission rate exists and constantly receives the cell.

[0012] In this case, if the physical layer devices are selected in accordance with the round robin scheduling, after the ATM layer device receives the cell from the plurality of physical layer devices having the low transmission rate, the ATM layer device receives the cell from the physical layer device having the high transmission rate.

[0013] Accordingly, before the physical layer device having the high transmission rate transmits the cell to the ATM layer device, it receives a next cell, so that there is possibility that a receiving buffer for temporarily storing the cells causes overflow.

[0014] Even if the receiving buffer does not cause the overflow, an actual transfer rate becomes smaller than an expected transfer rate because of a waiting time required for transferring the cell to the ATM layer device.

Summary of the Invention

[0015] Accordingly, it is an object of the present invention to provide an ATM layer device which has overcome the above mentioned problem of the prior art.

[0016] Another object of the present invention is to provide an ATM layer device capable of preventing the drop of the cell transfer rate and the overflow of the receiving buffer provided in the physical layer device.

[0017] The above and other objects of the present invention are achieved in accordance with the present invention by an ATM layer device controlling method realizing the function of an ATM layer by selecting one from a plurality of physical layer devices realizing the function of a physical layer, and executing a transfer of a cell, which is a unit of transmission, between the ATM layer device and the selected physical layer device, the method including the steps of holding the priority information indicating the previously set priority level of each of the plurality of physical layer devices, and selecting the physical layer device which should execute the cell transfer, in a predetermined order in accordance with the priority information.

[0018] At this time, it is possible to output the address of the physical layer device which should execute the cell transfer, selected in accordance with the priority information, and to execute the cell transfer between the ATM layer device and the physical layer device desig-

nated by the address. Alternatively. it is also possible to output the address of the physical layer device of a candidate which should execute the cell transfer, in accordance with the priority information. and to respond to a cell transfer enable notify signal indicating that the cell transfer is possible. outputted from the physical layer device designated by the address. so as to output the address of the physical layer device which should execute the cell transfer.

[0019] Preferably. the pnority is so set that the larger the transmission rate of the physical layer device is. the higher the priority level of the physical layer device is.

[0020] According to another aspect of the present invention there is provided an ATM layer device configured to realize the function of an ATM layer by selecting one from a plurality of physical layer devices realizing the function of a physical layer. and executing a transfer of a cell. which is a unit of transmission. between the ATM layer device and the selected physical layer device the ATM layer device including a priority information register holding the priority information indicating the previously set priority level of each of the plurality of physical layer devices. a selecting physical layer address output circuit for outputting the address of the physical layer device which should execute the cell transfer. in a predetermined order in accordance with the priority information. and a control circuit for executing the transfer of the cell between the ATM layer device and the physical layer device designated by the address

[0021] In one embodiment. the ATM layer device further includes a polling physical layer address output circuit for outputting. in the predetermined order, the address of the physical layer device of a candidate which should execute the cell transfer. selected in accordance with the priority information, and wherein the selecting physical layer address output circuit responds to a cell transfer enable notify signal indicating that the cell transfer is possible. outputted from the physical layer device designated from the address. so as to output the address of the physical layer device which should execute the cell transfer

[0022] Preferably. the selecting physical layer address output circuit can include a plurality of priority control registers for holding the information of the physical layer devices in units of different levels of the priority, and the polling physical layer address output circuit can include a plurality of priority control registers for holding the information of the physical layer devices in units of different levels of the priority.

[0023] Furthermore. it can be so set that the larger the transmission rate of the physical layer device is. the higher the priority level of the physical layer device is.

[0024] With the above mentioned arrangement. the ATM layer device in accordance with the present invention holds the priority information indicating the previously set priority level of each of a plurality of physical layer devices. and selects the physical layer device which should execute the cell transfer, in the predetermined order in accordance with the priority information Therefore. the higher the priority level of the physical layer device is. the larger the opportunity of the selection of the physical layer device becomes. so that the data transfer amount per a unit time, of the physical layer device having the high priority level, can be increased.

[0025] The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention with reference to the accompanying drawings.

Brief Description of the Drawings

[0026]

Fig. 1 is a block diagram illustrating the structure of the ATM layer device in accordance with the present invention:

Fig. 2 is a diagram illustrating one example of the content stored in the priority information register provided in the ATM layer device shown in Fig. 1:

Figs. 3A. 3B and 3C are diagrams respectively illustrating the contents of the first and fourth priority control registers. the contents of the second and fifth priority control registers. and the contents of the third and sixth priority control registers, provided in the ATM layer device shown in Fig 1:

Fig 4 is a diagram illustrating one example of the method for selecting the physical layer device by the ATM layer device in accordance with the present invention:

Fig. 5 is a flowchart illustrating the procedures of the processing in the polling physical layer address output circuit provided in the ATM layer device in accordance with the present invention:

Fig. 6 is a flowchart illustrating the procedures of the processing in the selecting physical layer address output circuit provided in the ATM layer device in accordance with the present invention:

Fig. 7 is a block diagram illustrating the connection between the ATM layer device and the physical layer devices: and

Fig. 8 is a block diagram illustrating the prior art method for selecting the physical layer device by the ATM layer device

Description of the Preferred embodiments

[0027] Now, the present invention will be described with reference to the accompanying drawings.

[0028] The ATM layer device in accordance with the present invention holds priority information indicating a previously set priority level of respective physical layer devices. and selects a physical layer device which should execute a cell transfer. in accordance with the priority information

[0029] In the following, only circuits which are provided in the ATM layer device and which realize the function of selecting the physical layer device, will be described. However, it would be a matter of course that the ATM layer device includes means for realizing the function of the cell multiplexing and the function of the cell separation, but since these means do not have a close relation to the present invention, these means are omitted in the drawing and explanation thereof will be omitted.

[0030] In addition, the connection between the ATM layer device and the physical layer devices is similar to the prior art (Fig. 7).

[0031] Fig. 1 is a block diagram illustrating the structure of the ATM layer device in accordance with the present invention.

[0032] As shown in Fig. 1, an ATM layer device 1 is connected to "n" physical layer devices 2_1 to 2n and a host controller 3 for generating a control signal for rewriting the priority information of the physical layer devices 2_1 to 2n.

[0033] The ATM layer device 1 outputs an address of the physical layer device (2_1 to 2n) which should execute the cell transfer, and on the other hand, each of the physical layer devices 2_1 to 2n outputs a cell transfer enable notify signal indicating whether or not the corresponding physical layer device can execute the cell transfer.

[0034] The ATM layer device 1 includes a priority information register 11 for holding the priority information of the respective physical layer devices 2_1 to 2n, a selecting physical layer address output circuit 12 for outputting a first physical layer address which is an address of the physical layer device which should execute the cell transfer (namely, the address of the selected physical layer device), a polling physical layer address output circuit 13 for outputting a second physical layer address which is an address of the physical layer device which is a candidate for selection, a first selector 14 for selecting either of the first physical layer address and the second physical layer address in accordance with a first selection signal outputted from the selecting physical layer address output circuit 12, and a second selector 15 for alternately outputting the physical layer address outputted from the first selector 14 and the data "1" (of the same bit number as that of the physical layer address) in accordance with a second selection signal supplied from a control circuit (not shown), in order to output the address signal defined in the UTOPIA interface.

[0035] The selecting physical layer address output circuit 12 includes a first priority control register 16_1 for holding the information of the physical layer devices having the highest priority, a second priority control register 16_2 for holding the information of the physical layer devices having a middle priority, and a third priority control register 16_3 for holding the information of the physical layer devices having the lowest priority.

[0036] Similarly, the polling physical layer address output circuit 13 includes a fourth priority control register 17_1 for holding the information of the physical layer devices having the highest priority, a fifth priority control register 17_2 for holding the information of the physical layer devices having a middle priority, and a sixth priority control register 17_3 for holding the information of the physical layer devices having the lowest priority.

[0037] Fig. 2 is a diagram illustrating one example of the content stored in the priority information register 11 shown in Fig. 1, Figs. 3A, 3B and 3C are diagrams illustrating the contents of the priority control registers shown in Fig. 1, Fig. 3A is a diagram illustrating the contents of the first and fourth priority control registers 16_1 and 17_1, Fig. 3B is a diagram illustrating the contents of the second and fifth priority control registers 16_2 and 17_2, and Fig. 3C is a diagram illustrating the contents of the third and sixth priority control registers 16_3 and 17_3.

[0038] As shown in Fig. 2, the priority information of each of the physical layer devices 2_1 to 2n is stored in the priority information register 11 in units of two bits.

[0039] In addition, as shown in Fig. 3A, in each of the first priority control register 16_1 and the fourth priority control register 17_1, the data "1" is written into the bit(s) corresponding to the physical layer device(s) having the highest priority.

[0040] Similarly, as shown in Fig. 3B, in each of the second priority control register 16_2 and the fifth priority control register 17_2, the data "1" is written into the bit(s) corresponding to the physical layer device(s) having the middle priority. As shown in Fig. 3C, in each of the third priority control register 16_3 and the sixth priority control register 17_3, the data "1" is written into the bit(s) corresponding to the physical layer device(s) having the lowest priority.

[0041] Incidentally, Fig. 2 and Figs. 3A, 3B and 3C illustrate the examples of the contents stored in the priority information register 11, the first to third priority control registers 16_1 to 1_{63} and the fourth to sixth priority control registers 17_1 to 17_3 in the case having 31 physical layer devices.

[0042] The priority control registers are provided in accordance with the number of priority levels. For example, when the priority has two levels (namely, a high priority and a low priority), it is sufficient if each of the selecting physical layer address output circuit 12 and the polling physical layer address output circuit 13 includes two priority control registers.

[0043] With the above mentioned arrangement, the priority information register 11 is previously written with the priority information as shown in Fig. 2, of the respective physical layer devices 2_1 to 2n, by the host controller 3.

[0044] The ATM layer device 1 firstly outputs from the polling physical layer address output circuit 13 the second physical layer address which is the address of the physical layer device of the selection candidate.

[0045] At this time, the selecting physical layer address output circuit 12 outputs the first selection signal causing the first selector 14 to output the second phys-

ical layer address. The second selector 15 alternately outputs the second physical layer address outputted from the first selector 14 and the data "1" of the bit number equal to that of the second physical layer address. in accordance with the second selection signal. so as to transmit it to the selecting physical layer address output circuit 12 and the physical layer devices 2_1 to 2n.

[0046] The physical layer device designated by the second physical layer address outputs the cell transfer enable notify signal indicating whether or not the cell transfer is possible, to the selecting physical layer address output circuit 12.

[0047] The selecting physical layer address output circuit 12 receives the second physical layer address outputted from the second selector 15 and the cell transfer enable notify signal outputted from the physical layer device designated by the second physical layer address. and outputs the address of the physical layer device which can execute the cell transfer (first physical layer address) and simultaneously outputs the first selection signal causing the first selector 14 to output the first physical layer address.

[0048] Succeedingly, the second selector 15 alternately outputs the first physical layer address outputted from the first selector 14 and the data "1" of the bit number equal to that of the first physical layer address, in accordance with the second selection signal, so as to transmit it to the selecting physical layer address output circuit 12 and the physical layer devices 2_1 to 2n.

[0049] The physical layer device designated by the first physical layer address executes the cell tranfer between the physical layer device designated by the second physical layer address and a control circuit (not shown) provided in the ATM layer device.

[0050] For example. now consider that, as shown in Fig. 4. the 31 physical layer devices are divided into the physical layer devices PHY0 and PHY3 having the highest priority. the physical layer devices PHY1 and PHY2 having the middle priority and the physical layer devices PHY4 to PHY30 having the lowest priority In this case. the physical layer devices are selected by in the order determined by a priority-based hierarchical combination of a loop constituted of the physical layer devices having the highest priority. another loop constituted of the physical layer devices having the middle priority. and still another loop constituted of the physical layer devices having the lowest priority. as in the named order of PHY0, PHY3. PHY1 PHY0. PHY3, PHY2. PHY0. PHY3. PHY4. PHY0. • • •.

[0051] Next. the procedures of the processing in the polling physical layer address output circuit 13 and the procedures of the processing in the selecting physical layer address output circuit 12 will be described with Figs. 5 and 6.

[0052] Fig. 5 is a flowchart illustrating the procedures of the processing in the polling physical layer address output circuit shown in Fig 1. Fig 6 is a flowchart illustrating the procedures of the processing in the selecting physical layer address output circuit shown in Fig. 1.

[0053] In the flowchart shown in Fig. 5, the polling physical layer address output circuit 13 firstly writes the priority information of the respective physical layer devices 2_1 to 2n to the fourth to sixth priority control registers 17_1 to 17_3 on the basis of the content of the priority information register 11 (step S1).

[0054] Next, the polling physical layer address output circuit 13 ascertains whether or not all the bits of the fourth priority control register 17_1 are "0" (step S2). If all the bits of the fourth priority control register 17_1 are not "0", the polling physical layer address output circuit 13 outputs the address of the physical layer device corresponding to the least significant bit of the "1"-written bits in the fourth priority control register 17_1 (the second physical layer address) (step S3).

[0055] Furthermore, the polling physical layer address output circuit 13 rewrites the bit of the fourth priority control register 17_1 corresponding to the physical layer device selected in the step S3, to "0" (step S4), and returns to the step 2 so as to repeat the processing of the steps S2 to S4 until all the bits of the fourth priority control register 17_1 become "0".

[0056] When all the bits of the fourth priority control register 17_1 are "0" in the step S2, the polling physical layer address output circuit 13 writes again the priority information of the corresponding physical layer devices (2_1 and 2_4 in the example of Fig. 4) to the fourth priority control register 17_1 on the basis of the content of the priority information register 11 (step S5).

[0057] After completion of the step S5. the processing goes into a step S6 in which the polling physical layer address output circuit 13 ascertains whether or not all the bits of the fifth priority control register 17_2 are "0". If all the bits of the fifth priority control register 17_2 are not "0", the polling physical layer address output circuit 13 outputs the address of the physical layer device corresponding to the least significant bit of the "1"-written bits in the fifth priority control register 17_2 (the second physical layer address) (step S7).

[0058] Furthermore. the polling physical layer address output circuit 13 rewrites the bit of the fifth priority control register 17_2 corresponding to the physical layer device selected in the step S7, to "0" (step S8), and returns to the step 2.

[0059] On the other hand. if all the bits of the fifth priority control register 17_2 are "0" in the step S6. the polling physical layer address output circuit 13 writes again the priority information of the corresponding physical layer devices (2_2 and 2_3 in the example of Fig. 4) to the fifth priority control register 17_2 on the basis of the content of the priority information register 11 (step S9).

[0060] After completion of the step S9. the processing goes into a step S10 in which the polling physical layer address output circuit 13 ascertains whether or not all the bits of the sixth priority control register 17_3 are "0" If all the bits of the sixth priority control register 17_3 are

not "0", the polling physical layer address output circuit 13 outputs the address of the physical layer device corresponding to the least significant bit of the "1"-written bits in the sixth priority control register 17_3 (the second physical layer address) (step S11).

[0061] Furthermore, the polling physical layer address output circuit 13 rewrites the bit of the sixth priority control register 17_3 corresponding to the physical layer device selected in the step S11, to "0" (step S12), and returns to the step 2.

[0062] On the other hand, if all the bits of the sixth priority control register 173 are "0" in the step S10, the polling physical layer address output circuit 13 writes again the priority information of the corresponding physical layer devices (2_5 to 2n in the example of Fig. 4) to the sixth priority control register 17_3 on the basis of the content of the priority information register 11 (step S13). Therefore, the processing returns to the step S2, so that the processing of the steps S2 to S13 is repeated.

[0063] With the above mentioned processing, the polling physical layer address output circuit 13 outputs the physical layer address in the order determined by the priority-based hierarchical combination of a high priority loop composed of the physical layer devices having the highest priority, a middle priority loop composed of the physical layer devices having the middle priority, and a low priority loop composed of the physical layer devices having the lowest priority, as shown in Fig. 4.

[0064] In the flow chart shown in Fig 6, the selecting physical layer address output circuit 12 firstly writes the priority information of the respective physical layer devices 2_1 to 2n into the first, second and third priority control registers 16_1 to 16_3 on the basis of the content of the priority information register 11 (step S21).

[0065] Then, the selecting physical layer address output circuit 12 ascertains whether or not all the contents of the first priority control register 16_1 are "0" (step S22), when all the contents of the first priority control register 16_1 are not "0", the selecting physical layer address output circuit 12 ascertains whether or not the physical layer device corresponding to the least significant bit of the "1"-written bits can execute the cell transfer (step S23). Whether or not the cell transfer is executable, is discriminated on the basis of the second physical layer address and the cell transfer enable notify signal outputted from the physical layer device designated by the second physical layer address.

[0066] When the result of the processing in the step S23 indicates that the cell transfer is possible, the selecting physical layer address output circuit 12 outputs the address of the corresponding physical layer device (first physical layer address), so that the cell transfer is executed between the ATM layer device and the corresponding physical layer device (step S24). On the other hand, when the cell transfer is not possible, or when the processing in the step S24 is completed, the selecting physical layer address output circuit 12 rewrites the least significant bit of the "1"-written bits in the first priority control register 16_1 to "0" (step S25), and the processing returns to the step S22 so that the processing of the steps S22 to S25 is repeated until all the contents of the first priority control register 16_1 become "0".

[0067] On the other hand, if all the bits of the first priority control register 161 are "0" in the step S22, the selecting physical layer address output circuit 12 writes again the priority information of the corresponding physical layer devices (2_1 and 2_4 in the example of Fig. 4) to the first priority control register 16_1 on the basis of the content of the priority information register 11 (step S26).

[0068] After completion of the step S26, the processing goes into a step S27 in which the selecting physical layer address output circuit 12 ascertains whether or not all the bits of the second priority control register 16_2 are "0". If all the bits of the second priority control register 16_2 are not "0", the selecting physical layer address output circuit 12 ascertains whether or not the physical layer device corresponding to the least significant bit of the "1"-written bits can execute the cell transfer (step S28). When the result of the processing in the step S28 indicates that the cell transfer is possible, the selecting physical layer address output circuit 12 outputs the address of the corresponding physical layer device (first physical layer address), so that the cell transfer is executed between the ATM layer device and the corresponding physical layer device (step S29). On the other hand, when the cell transfer is not possible, or when the processing in the step S29 is completed the selecting physical layer address output circuit 12 rewrites the least significant bit of the "1"-written bits in the second priority control register 16_2 to "0" (step S30), and the processing returns to the step S22.

[0069] On the other hand, if all the bits of the second priority control register 16_2 are "0" in the step S27, the selecting physical layer address output circuit 12 writes again the priority information of the corresponding physical layer devices (2_2 and 2_3 in the example of Fig. 4) to the second priority control register 16_2 on the basis of the content of the priority information register 11 (step S31).

[0070] After completion of the step S31, the processing goes into a step S32 in which the selecting physical layer address output circuit 12 ascertains whether or not all the bits of the third priority control register 16_3 are "0". If all the bits of the third priority control register 16_3 are not "0", the selecting physical layer address output circuit 12 ascertains whether or not the physical layer device corresponding to the least significant bit of the "1"-written bits can execute the cell transfer (step S33). When the result of the processing in the step S33 indicates that the cell transfer is possible, the selecting physical layer address output circuit 12 outputs the address of the corresponding physical layer device (first physical layer address), so that the cell transfer is executed between the ATM layer device and the corresponding physical layer device (step S34) On the other hand, when the cell transfer is not possible, or when the

processing in the step S34 is completed, the selecting physical layer address output circuit 12 rewrites the least significant bit of the "1"-written bits in the third priority control register 16_3 to "0" (step S35), and the processing returns to the step S22.

[0071] On the other hand, if all the bits of the third priority control register 16_3 are "0" in the step S32, the selecting physical layer address output circuit 12 writes again the priority information of the corresponding physical layer devices (2_5 to 2n in the example of Fig. 4) to the third priority control register 16_3 on the basis of the content of the priority information register 11 (step S36), and the processing returns to the step S22, so that the processing of the steps S22 to S36 is repeated.

[0072] With the above mentioned processing, the selecting physical layer address output circuit 12 outputs the physical layer address in the order determined by the priority-based hierarchical combination of a high priority loop composed of the physical layer devices having the highest priority, a middle priority loop composed of the physical layer devices having the middle priority, and a low priority loop composed of the physical layer devices having the lowest priority, as shown in Fig. 4.

[0073] As seen from the above, the ATM layer device in accordance with the present invention holds the priority information indicating the previously set priority level of each of a plurality of physical layer devices, and selects the physical layer device which should execute the cell transfer, in the predetermined order in accordance with the priority information. Therefore, the higher the priority level of the physical layer device is, the larger the opportunity of the selection of the physical layer device becomes, so that the data transfer amount per a unit time, of the physical layer device having the high priority level, can be increased.

[0074] In particular, by giving a high priority to the physical layer device having a high transmission rate, it is possible to suppress the overflow of the receiving buffer in the physical layer device having the high transmission rate.

[0075] The invention has thus been shown and described with reference to the specific embodiments. However, it should be noted that the present invention is in no way limited to the details of the illustrated structures but changes and modifications may be made.

Claims

1. An ATM layer device controlling method realizing the function of an ATM layer by selecting one from a plurality of physical layer devices realizing the function of a physical layer, and executing a transfer of a cell, which is a unit of transmission, between the ATM layer device and the selected physical layer device, the method including the steps of holding the priority information indicating the previously set priority level of each of said plurality of physical layer devices, and selecting the physical layer device which should execute the cell transfer, in a predetermined order in accordance with the priority information.

2. A method claimed in Claim 1 further including the steps of outputting the address of the physical layer device which should execute the cell transfer, selected in accordance with the priority information, and executing the cell transfer between the ATM layer device and the physical layer device designated by said address.

3. A method claimed in Claim 2 further including the steps of outputting the address of the physical layer device of a candidate which should execute the cell transfer, in accordance with the priority information, and responding to a cell transfer enable notify signal indicating that the cell transfer is possible, outputted from the physical layer device designated by said address, so as to output the address of the physical layer device which should execute the cell transfer.

4. A method claimed in any of Claims 1 to 3 wherein the larger the transmission rate of the physical layer device is, the higher the priority level of the physical layer device is.

5. An ATM layer device configured to realize the function of an ATM layer by selecting one from a plurality of physical layer devices realizing the function of a physical layer, and executing a transfer of a cell, which is a unit of transmission, between the ATM layer device and the selected physical layer device, the ATM layer device including a priority information register holding the priority information indicating the previously set priority level of each of said plurality of physical layer devices, a selecting physical layer address output circuit for outputting the address of the physical layer device which should execute the cell transfer, in a predetermined order in accordance with the priority information, and a control circuit for executing the transfer of the cell between the ATM layer device and the physical layer device designated by said address.

6. An ATM layer device claimed in Claim 5 further including a polling physical layer address output circuit for outputting, in said predetermined order, the address of the physical layer device of a candidate which should execute the cell transfer, selected in accordance with the priority information, and wherein said selecting physical layer address output circuit responds to a cell transfer enable notify signal indicating that the cell transfer is possible, outputted from the physical layer device designated from said address so as to output the address of the physical layer device which should execute the

cell transfer.

7. An ATM layer device claimed in Claim 5 or 6, wherein said selecting physical layer address output circuit includes a plurality of priority control registers for holding the information of said physical layer devices in units of different levels of the priority.

8. An ATM layer device claimed in Claim 6 or 7, wherein said polling physical layer address output circuit includes a plurality of priority control registers for holding the information of said physical layer devices in units of different levels of the priority.

9. An ATM layer device claimed in any of Claims 5 to 8 wherein the larger the transmission rate of the physical layer device is, the higher the priority level of the physical layer device is.

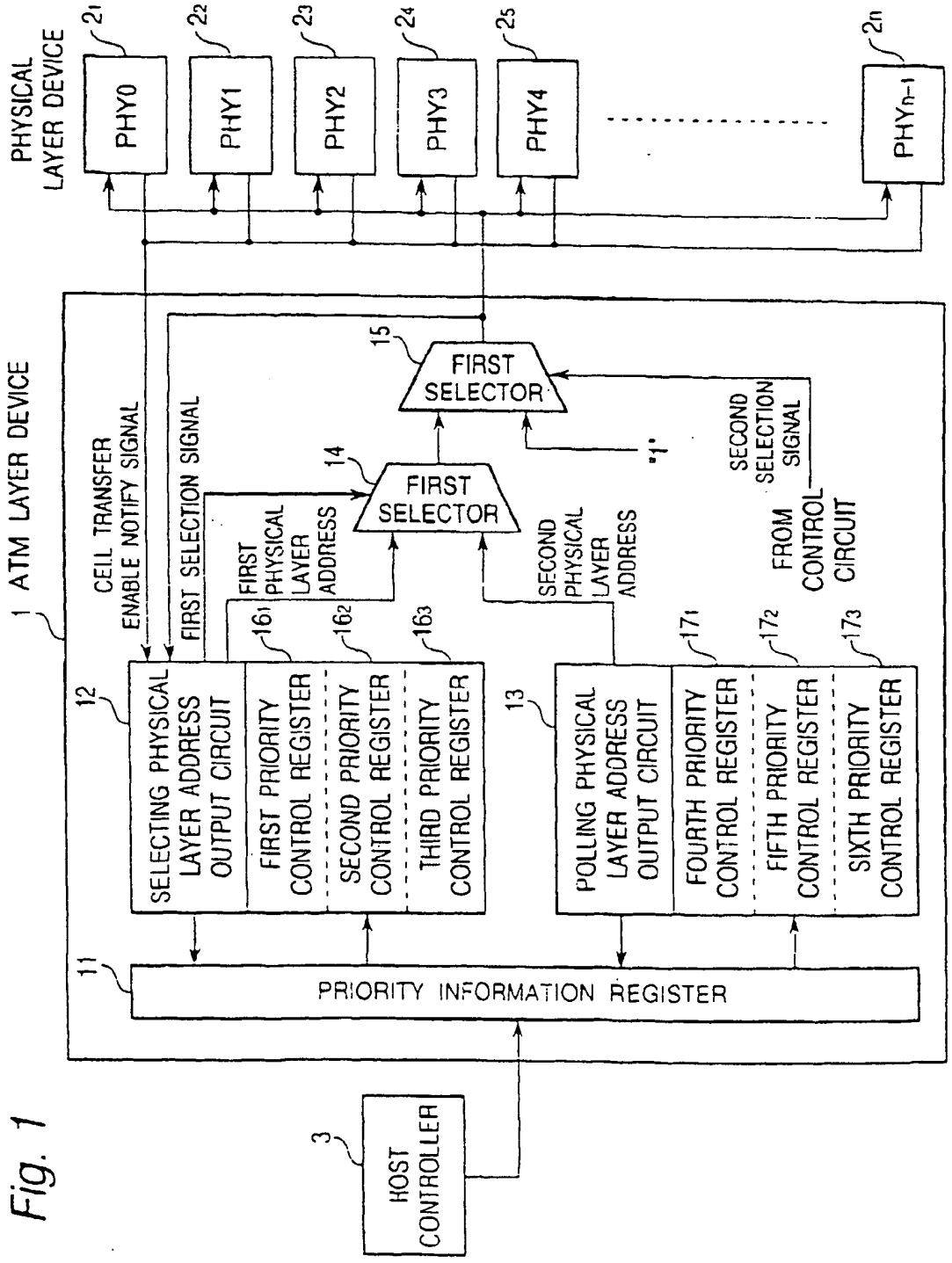

PHYSICAL LAYER DEVICE
PHY0
PHY1
PHY2
PHY3
PHY4
PHYn-1
21
22
23
24
25
2n
1 ATM LAYER DEVICE
CELL TRANSFER ENABLE NOTIFY SIGNAL
FIRST SELECTION SIGNAL
15
FIRST SELECTOR
14
FIRST SELECTOR
"1"
SECOND SELECTION SIGNAL
FIRST PHYSICAL LAYER ADDRESS
SECOND PHYSICAL LAYER ADDRESS
FROM CONTROL CIRCUIT
12
SELECTING PHYSICAL LAYER ADDRESS OUTPUT CIRCUIT
FIRST PRIORITY CONTROL REGISTER
SECOND PRIORITY CONTROL REGISTER
THIRD PRIORITY CONTROL REGISTER
161
162
163
13
POLLING PHYSICAL LAYER ADDRESS OUTPUT CIRCUIT
FOURTH PRIORITY CONTROL REGISTER
FIFTH PRIORITY CONTROL REGISTER
SIXTH PRIORITY CONTROL REGISTER
171
172
173
11
PRIORITY INFORMATION REGISTER
3
HOST CONTROLLER

Fig. 1

Fig. 2

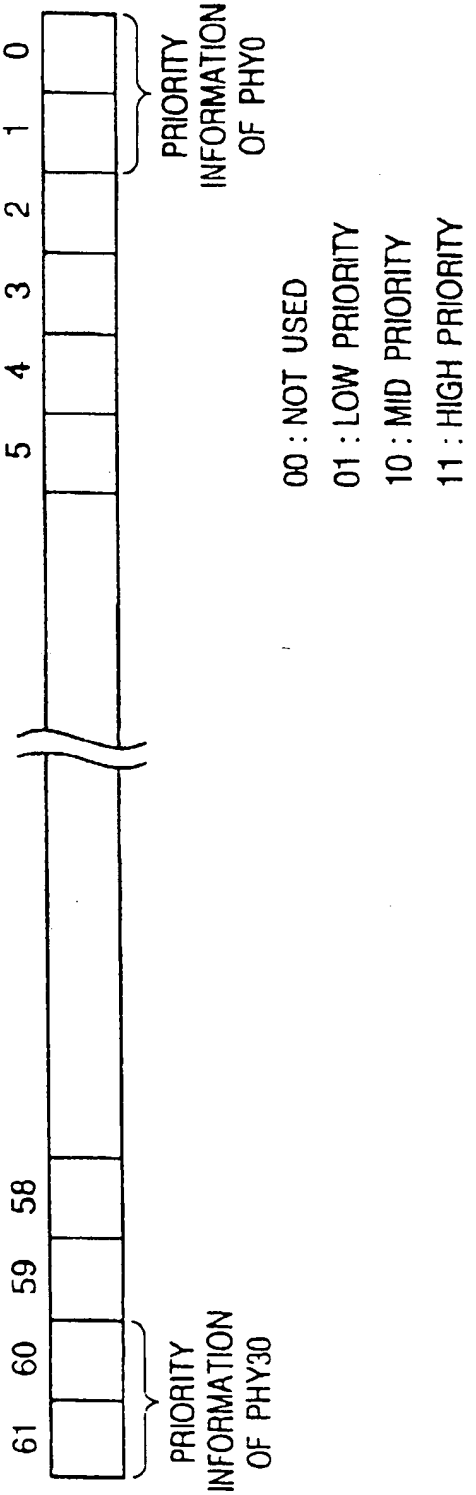
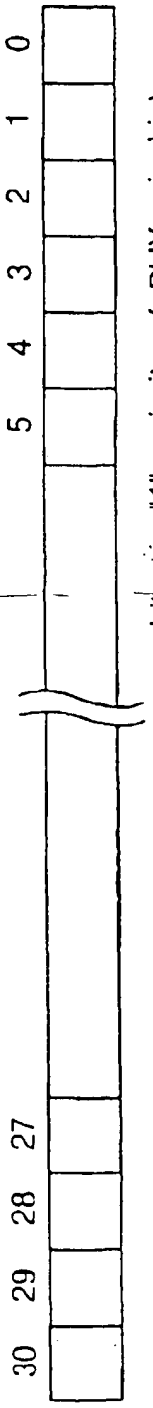
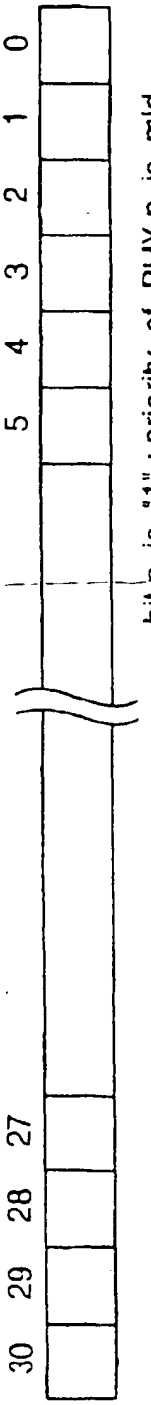

0
1
2
3
4
5
58
59
60
61
PRIORITY INFORMATION OF PHY0
PRIORITY INFORMATION OF PHY30
00 : NOT USED
01 : LOW PRIORITY
10 : MID PRIORITY
11 : HIGH PRIORITY

Fig. 3A



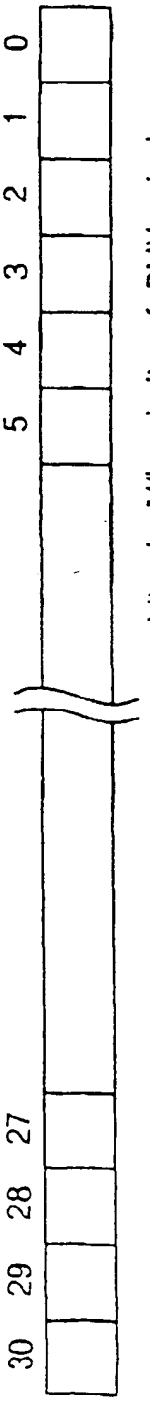
bit n is "1" : priority of PHY n is high
bit n is "0" : priority of PHY n is not high

Fig. 3B



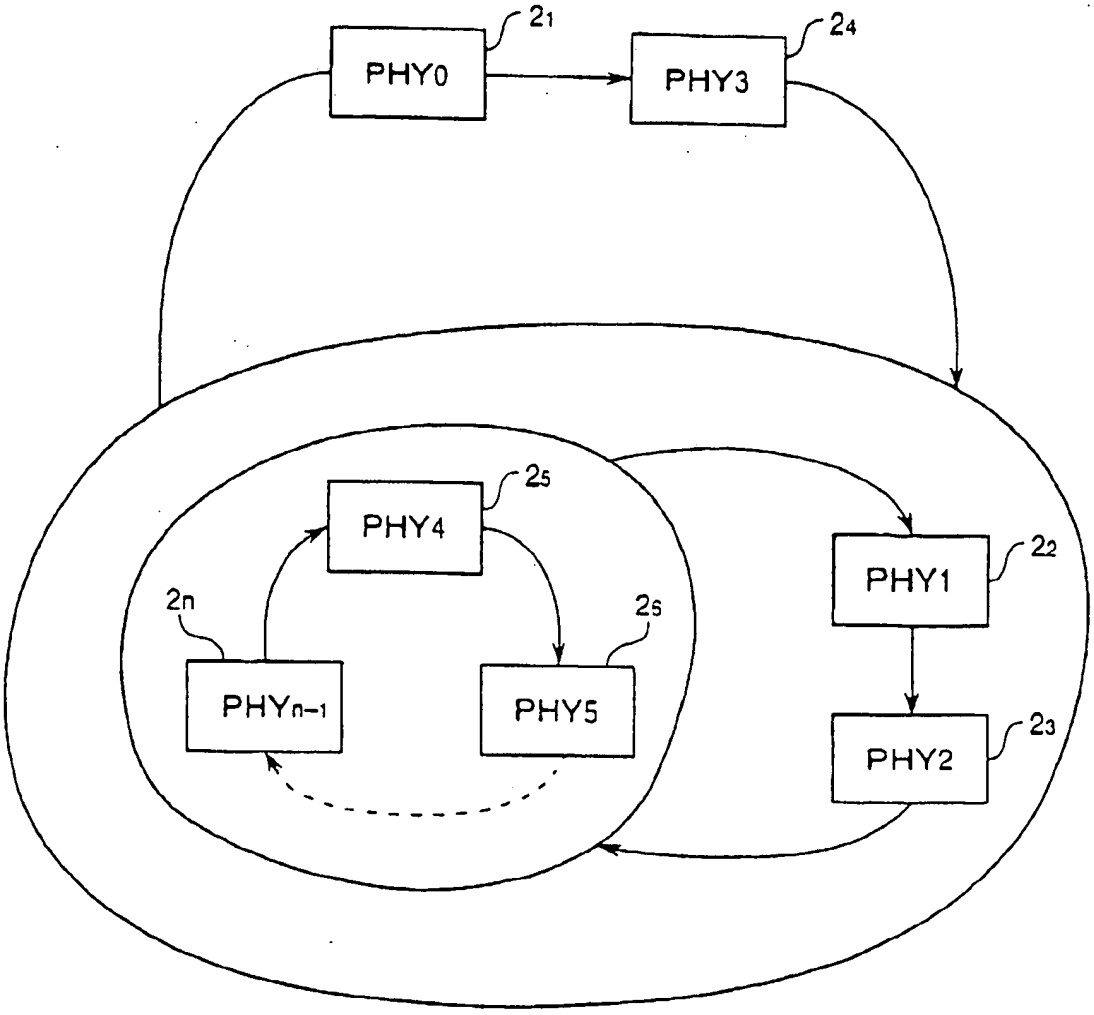
bit n is "1" : priority of PHY n is mid
bit n is "0" : priority of PHY n is not mid

Fig. 3C



bit n is "1" : priority of PHY n is low
bit n is "0" : priority of PHY n is not low

Fig. 4



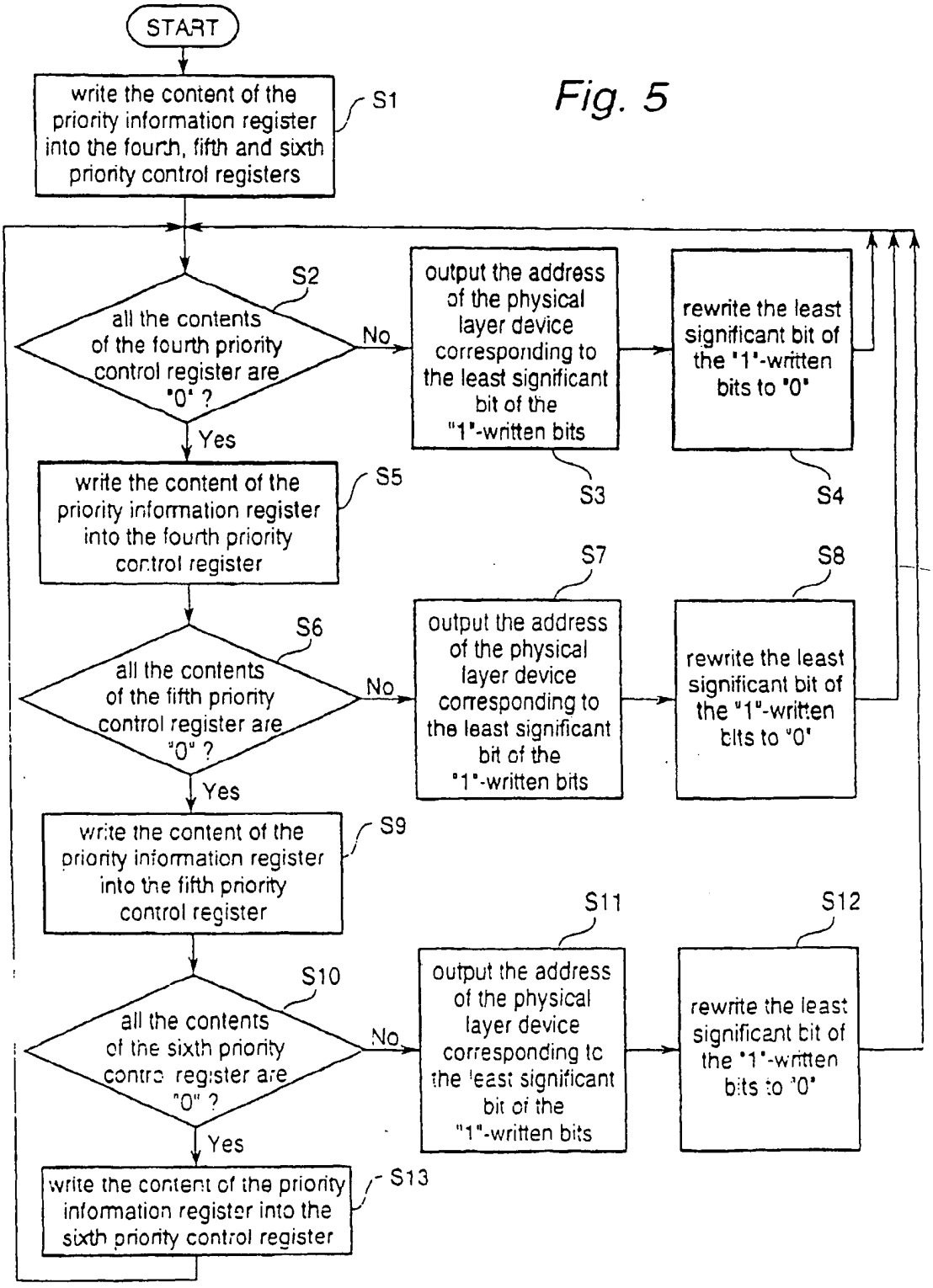

START
write the content of the priority information register into the fourth, fifth and sixth priority control registers
S1
S2
all the contents of the fourth priority control register are "0" ?
No
Yes
output the address of the physical layer device corresponding to the least significant bit of the "1"-written bits
S3
rewrite the least significant bit of the "1"-written bits to "0"
S4
write the content of the priority information register into the fourth priority control register
S5
S6
all the contents of the fifth priority control register are "0" ?
No
Yes
S7
output the address of the physical layer device corresponding to the least significant bit of the "1"-written bits
S8
rewrite the least significant bit of the "1"-written bits to "0"
write the content of the priority information register into the fifth priority control register
S9
S10
all the contents of the sixth priority control register are "0" ?
No
Yes
S11
output the address of the physical layer device corresponding to the least significant bit of the "1"-written bits
S12
rewrite the least significant bit of the "1"-written bits to "0"
write the content of the priority information register into the sixth priority control register
S13

Fig. 5

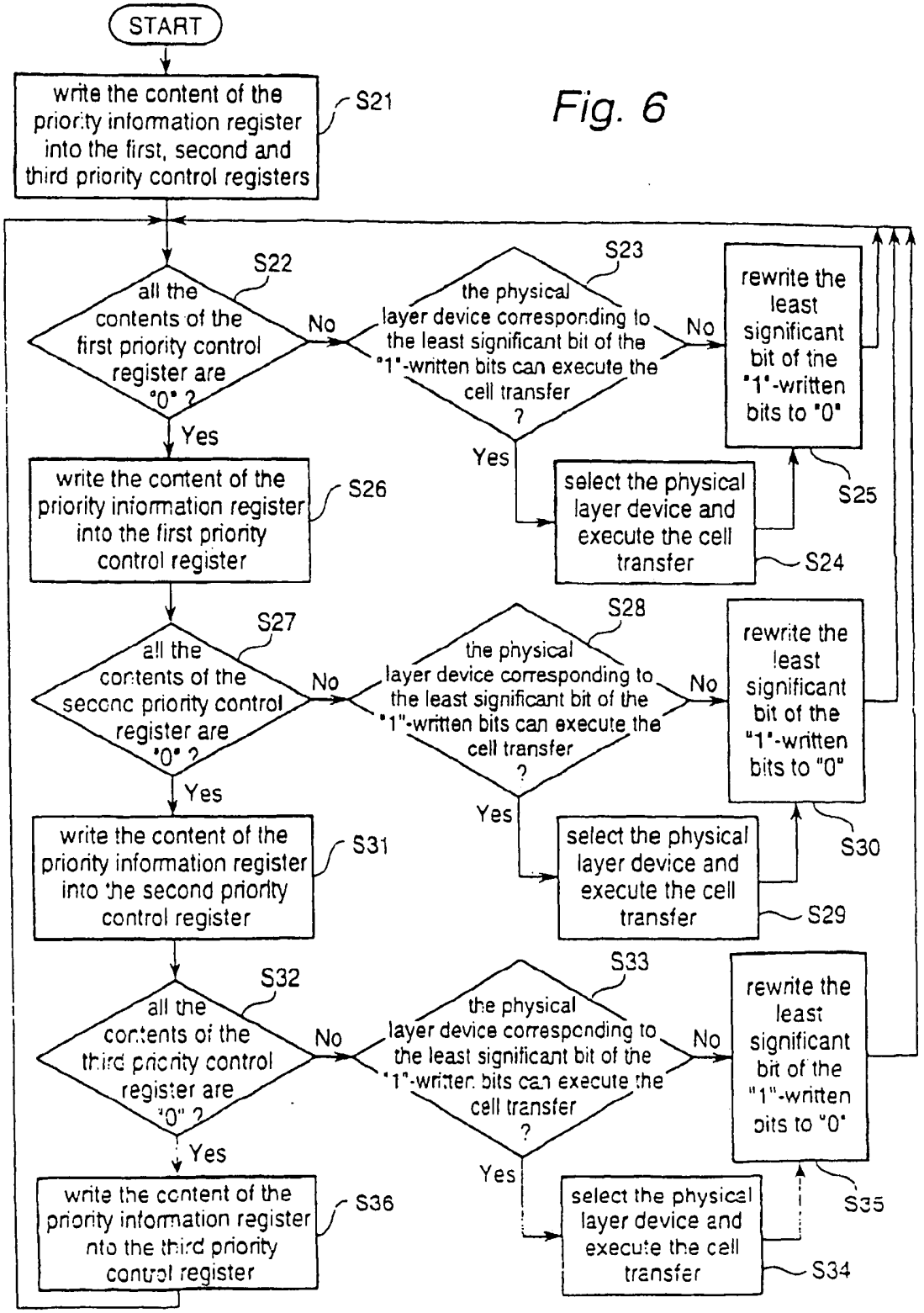


Fig. 6

Fig. 7 PRIOR ART

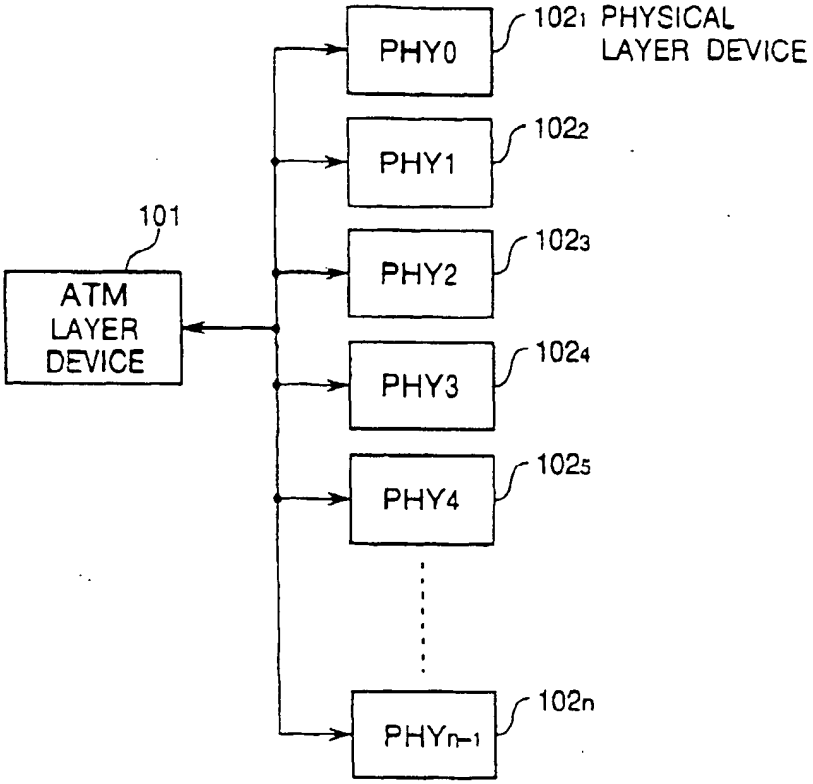


Fig. 8 PRIOR ART